



Extreme Statistics in Nanoscale Memory Design (Integrated Circuits and Systems)

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Knowledge exists: you only have to find it. VLSI design has come to an important inflection point with the appearance of large manufacturing variations as semiconductor technology has moved to 45 nm feature sizes and below. If we ignore the random variations in the manufacturing process, simulation-based design essentially becomes useless, since its predictions will be far from the reality of manufactured ICs. On the other hand, using design margins based on some traditional notion of worst-case scenarios can force us to sacrifice too much in terms of power consumption or manufacturing cost, to the extent of making the design goals even infeasible. We absolutely need to explicitly account for the statistics of this random variability, to have design margins that are accurate so that we can find the optimum balance between yield loss and design cost. This discontinuity in design processes has led many researchers to develop effective methods of statistical design, where the designer can simulate not just the behavior of the nominal design, but the expected statistics of the behavior in manufactured ICs. Memory circuits tend to be the hardest hit by the problem of these random variations because of their high replication count on any single chip, which demands a very high statistical quality from the product. Requirements of 5–6σ (0.

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